

SYSTEMS AND METHODS FOR REDUCING STATIC AND TOTAL POWER
CONSUMPTION IN A PROGRAMMABLE LOGIC DEVICE

Abstract of the Invention

[0058] A method and system for reducing power
5 consumption in a programmable logic device (PLD) is
provided. The power consumption may be reduced by
preferably continually considering power consumption as
a factor in circuit design during the technology
mapping, routing, and period following routing of the
10 programmable logic device.